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DENSE CONTENT ADDRESSABLE MEMORY CELL

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation in part of U.S. *now abandoned*
Application No. 10/127,175, filed April 22, 2002, in
the name of Morteza C. Afghahi, and a continuation-in-
part of U.S. Application No. 10/375,880, filed
now Patent No. 6,751,112
February 26, 2003, in the name of Morteza C. Afghahi,
which is a continuation-in-part of U.S. Application
now abandoned
No. 10/127,175, filed April 22, 2002, and claims the
benefit of the provisional application no. 60/448,551,
filed February 19, 2003, entitled "Dense Content
Addressable Memory Cell."

[0015] Transistors 26 and 27 can be operated in three different modes of operation:

[0016] a cutoff mode in which no current flows from source to drain (with the possible exception of a very small reverse current) and in which changes in the gate to drain voltage do not further reduce current flow;

[0017] a saturation mode in which the current flowing from source to drain is at a maximum value limited by the external resistance in the circuit and in which changes in the gate to drain voltage do not further increase current flow; and

[0018] a triode mode in which the drain current is at values between the current flow during cutoff and saturation and in which the amount of drain current flow is regulated by changes in the gate to drain voltage.

[0019] Examples of the process corners used during manufacture of the memory cell are as follows: The slow-fast
NMOS is slow and PMOS is fast (SF corner). In this SF

TP

corner, the sub-threshold leakage current of the NMOS is an order of magnitude more than typical NMOS sub-threshold leakage current, and the sub-threshold leakage current of the PMOS is an order of magnitude less than typical PMOS sub-threshold leakage current. The range of difference is magnified by environmental temperatures typically encountered in commercial applications of memory cells. Higher temperature results in higher leakage. For example, for every 10 degrees C increase in environmental temperature, the

TP ^{fast-slow} leakage current may double. For an FS corner, where ^{slow} NMOS is fast and PMOS is slow, the situation is reversed; that is, the sub-threshold leakage current of NMOS is lower than typical and the sub-threshold leakage current of PMOS is higher than typical.

[0020] Examples of environmental temperatures for which memory cells are designed for commercial applications typically vary in a range of -10 degrees C to 125 degrees C. Considering this temperature range

TP ^{slow-fast} _{fast-slow} and going from ^{slow} SF to ^{fast} FS, the ratio of NMOS leakage